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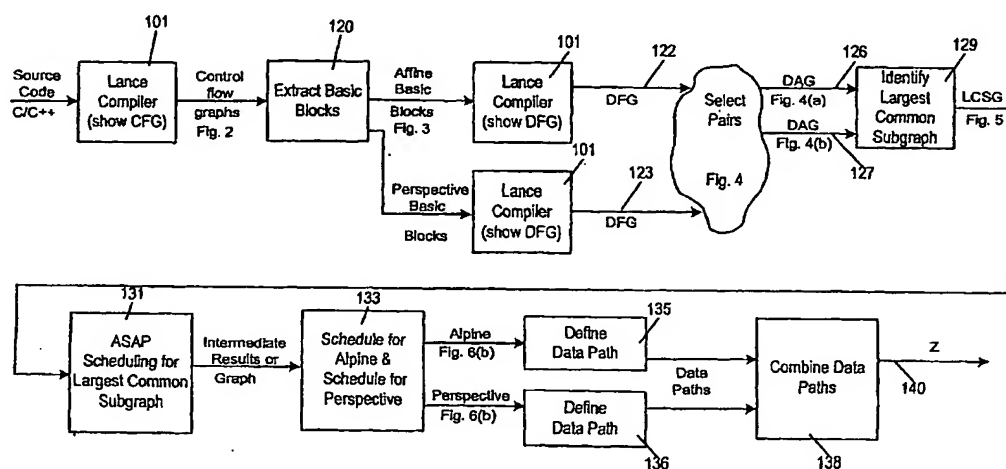
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(54) Title: RECONFIGURABLE PROCESSING



(57) Abstract: A method of producing a reconfigurable circuit device for running a computer program of moderate complexity such as multimedia processing. Code for the application is compiled into Control Flow Graphs representing distinct parts of the application to be run. (101, 120) From those Control Flow Graphs are extracted basic blocks (120). The basic blocks are converted to Data Flow Graphs by a compiler utility. From two or more Data Flow Graphs, a largest common subgraph is determined (129). The largest common subgraph is ASAP scheduled and substituted back into the Data Flow Graphs which also have been scheduled (131). The separate Data Flow Graphs containing the scheduled largest common subgraph are converted to data paths that are then combined to form code for operating the application (138). The largest common subgraph is effected in hardware that is shared among the parts of the application from which the Data Flow Graphs were developed. Scheduling of the overall code is effected for sequencing, providing fastest run times and the code is implemented in hardware by partitioning and placement of processing elements on a chip and design of the connective fabric for the design elements.



GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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## A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G06F 9/45, 17/50

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According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
EAST BRS; IEEE; ACM; CiteSeer.com

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JANSSEN et al. A Specification Invariant Technique for Regularity Improvement between Flow-Graph Clusters* IEEE Proceedings of the 1996 European Design and Test Conference (ED&TC) 1996, pages 138-143, especially Abstract, sections 1 and 4 (all).	1-11
A	BRISK et al. Instruction Generation and Regularity Extraction for Reconfiguration Processors ACM CASES 2002 October 2002, pages 1-8.	1-11
A	MOREANO et al. Datapath Merging and Interconnection Sharing for Reconfigurable Architectures ACM ISSS'02 October 2002, pages 38-43.	1-11
A	KAPLAN et al. Area-Efficient Instruction Set Synthesis for Reconfigurable System-on-Chip Designs ACM DAC 2004 June 2004, pages 395-400.	1-11

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

\* Special categories of cited documents:

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